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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/730,335	12/04/2000	Charles H. Dennison	MI22-1577	8465

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EXAMINER

NADAV, ORI

ART UNIT

PAPER NUMBER

2811

DATE MAILED: 02/26/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Applicati n No.

09/730,335

Applicant(s)

DENNISON, CHARLES H.

Examiner

ori nadav

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 January 2002.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 57-77 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 57-77 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

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DETAILED ACTION

1. The preliminary amendment filed on 03/26/2001 has been entered.

Oath/Declaration

2. The oath/declaration filed on 01/02/98 is acceptable.

Drawings

3. The formal drawings filed on 01/02/1998 are acceptable.

Information Disclosure Statement

4. The Information Disclosure Statement filed on 12/4/2000 has been considered.

Specification

5. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.
6. The abstract of the disclosure is objected to because the abstract should be brief, no longer than 150 words. Correction is required. See MPEP § 608.01(b).

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Claim Objections

7. Claims 57 and 62 are objected to because of the following informalities: the phrase "to diffusion", as recited in claims 57 and 62 is grammatically incorrect, and this unclear as to what is it meant.
8. Claims 76 and 77 recite the limitation "the silicide layer" in lines 1 and 2, respectively. There is insufficient antecedent basis for this limitation in the claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

9. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.
10. Claims 66 and 68 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 62 recites a semiconductive material being in electrical connection with the gate. There is no support for a

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semiconductive material within the insulating material does not contact the conductive diffusion barrier layer of the gate, as recited in claim 68.

11. There is no support for a silicide layer and a conductive diffusion barrier layer comprise the same material, as recited in claim 66.

Claim Rejections - 35 USC § 102

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

13. Claim 58 is rejected under 35 U.S.C. 102(e) as being anticipated by Thakur et al. (5,969,983).

Thakur et al. teach in figure 3 a field effect transistor comprising: a pair of source/drain regions 42 having a channel region positioned therebetween; and a gate 52 positioned operatively proximate the channel region, the gate comprising semiconductive material 58 conductively doped with at least one of a p-type or n-type conductivity enhancing

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impurity effective to render the semiconductive material electrically conductive, a silicide layer 54 and a conductive diffusion barrier layer 56 to diffusion of p-type or n-type conductivity enhancing impurity, the conductive diffusion barrier layer comprising TiWxNy, WxNy.

Although Thakur et al. do not explicitly state that the semiconductive material is conductively doped with at least one of a p-type or n-type conductivity, this feature is inherent in Thakur et al.'s device, because it is notoriously well known that the polysilicon is made to be conductivity doped in order to make a functional MOSFET.

14. Claim 58 is rejected under 35 U.S.C. 102(b) as being anticipated by Chow et al. (4,847,111).

Chow et al. teach in figure 1c a field effect transistor comprising: a pair of source/drain regions 15 having a channel region positioned therebetween; and a gate 21 positioned operatively proximate the channel region, the gate comprising semiconductive material 21 conductively doped with at least one of a p-type or n-type conductivity enhancing impurity effective to render the semiconductive material electrically conductive, a silicide layer 25b and a conductive diffusion barrier layer 25a to diffusion of p-type or n-type conductivity enhancing impurity, the conductive diffusion barrier layer comprising TiWxNy, WxNy.

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Although Chow et al. do not explicitly state that the semiconductive material conductively is doped with at least one of a p-type or n-type conductivity, this feature is inherent in Chow et al.'s device, because it is notoriously well known that the polysilicon is made to be conductivity doped in order to make a functional MOSFET.

15. Claim 59 is rejected under 35 U.S.C. 102(e) as being anticipated by Ku (5,856,237).

Ku teaches in figure 4F a field effect transistor comprising: a pair of source/drain regions 112 having a channel region positioned therebetween; and a gate positioned operatively proximate the channel region, the gate comprising semiconductive material 118 conductively doped with at least one of a p-type or n-type conductivity enhancing impurity effective to render the semiconductive material electrically conductive, a silicide layer 124 and a conductive diffusion barrier layer 140 to diffusion of p-type or n-type conductivity enhancing impurity, the conductive diffusion barrier layer comprising TiW_xNy, TiO_xNy.

Although Ku does not explicitly state that the semiconductive material conductively is doped with at least one of a p-type or n-type conductivity, this feature is inherent in Ku's device, because it is notoriously well known that the polysilicon is made to be conductivity doped in order to make a functional MOSFET.

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16. Claims 62, 63, 67 and 70 are rejected under 35 U.S.C. 102(b) as being anticipated by Pfister (4,997,785).

Pfister teaches in figure 7 an Integrated circuitry comprising: a field effect transistor including a gate, a gate dielectric layer, source/drain regions 24, 26 and a channel region; the gate comprising semiconductive material 16 conductively doped with a conductivity enhancing impurity of a first type N⁺ and a conductive diffusion barrier layer 30 to diffusion of first or second type conductivity enhancing impurity; and insulative material 44 received proximate the gate, the insulative material including semiconductive material 20 provided therein in electrical connection with the gate, the semiconductive material provided within the insulative material being conductively doped with a conductivity enhancing impurity of a second type P⁺, the conductive diffusion barrier layer of the gate being provided between the gate semiconductive material and the semiconductive material provided within the insulative material, wherein the semiconductive material within the insulating material contacts the conductive diffusion barrier layer of the gate, and wherein the conductive diffusion barrier layer is received over the gate semiconductive material, and the semiconductive material within the insulating material is received over the gate.

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Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

18. Claims 57 and 60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ku in view of Visokay et al. (6,211,034) and Igarashi (6,107,656).

Ku teaches substantially the entire claimed structure, as applied to claim 59 above, including a conductive diffusion barrier layer comprising TiN formed over the silicide layer, but except conductive diffusion barrier layer comprising TiWxNy

Visokay et al. teach a conductive diffusion barrier layer comprising TiN or TiWxNy (column 9, lines 3-7).

Igarashi teaches a gate electrode comprising TiN or TiWxNy (column 4, lines 4-9).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a conductive diffusion barrier layer comprising TiWxNy in Ku's gate electrode, because TiN and TiWxNy are conventional interchangeable materials used as conductive barrier diffusion layers in a gate electrode.

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19. Claims 57 and 61 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bai et al. (5,818,092) in view of Visokay et al. (6,211,034) and Igarashi (6,107,656).

Bai et al. teach in figure 2C a field effect transistor comprising: a pair of source/drain regions 216 having a channel region positioned therebetween; and a gate positioned operatively proximate the channel region, the gate comprising semiconductive material 204 conductively doped with at least one of a p-type or n-type conductivity enhancing impurity effective to render the semiconductive material electrically conductive, a silicide layer 220 and a conductive diffusion barrier layer 206 to diffusion of p-type or n-type conductivity enhancing impurity, the conductive diffusion barrier layer comprising TiN (column 4, lines 18-19) formed under the silicide layer 220.

Bai et al. do not teach conductive diffusion barrier layer comprising TiWxNy.

Visokay et al. teach a conductive diffusion barrier layer comprising TiN or TiWxNy (column 9, lines 3-7).

Igarashi teaches a gate electrode comprising TiN or TiWxNy (column 4, lines 4-9).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a conductive diffusion barrier layer comprising TiWxNy in Bai et al.'s gate electrode, because TiN and TiWxNy are conventional interchangeable materials used as conductive barrier diffusion layers in a gate electrode.

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20. Claim 64 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pfiester.

Pfiester teaches in figure 7 substantially the entire claimed structure, as applied to claim 62 above, except a first type is p and a second type is n.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a first type p and a second type n in Pfiester's device, because it is conventional to reverse the polarity of the transistor.

21. Claims 65, 66, 69, and 72-76, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Pfiester in view of Ku.

Pfiester teaches in figure 7 substantially the entire claimed structure, as applied to claim 62 above, except a gate also comprises a conductive silicide.

Ku teaches in figure 4F a gate comprises a conductive diffusion barrier layer 140 selected from the group consisting of W_xN_y , TiO_xN_y , and TiW_xN_y , and mixtures thereof over a conductive silicide 124.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a gate also comprises a conductive silicide in Pfiester's device, in order to reduce the contact resistance of the gate.

22. Claims 68 and 77, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Pfiester in view of Bai et al.

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Pfiester teaches in figure 7 substantially the entire claimed structure, as applied to claim 62 above, except a gate also comprises a conductive silicide.

Bai et al. teach in figure 2C a gate comprises a conductive diffusion barrier layer 206 under a conductive silicide 220.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a gate also comprises a conductive silicide in Pfiester's device, in order to reduce the contact resistance of the gate.

Regarding claim 68, the device of Pfiester and Bai et al. comprises a conductive silicide over the conductive diffusion barrier layer. Therefore, the semiconductive material within the insulating material does not contact the conductive diffusion barrier layer of the gate.

23. Claim 71 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pfiester in view of Kimura (5,883,418)..

Pfiester teaches in figure 7 substantially the entire claimed structure, as applied to claim 62 above, except the insulative material comprises an opening substantially void of any conductive diffusion barrier layer material.

Kimura teaches in figure 1 an insulative material 20 comprises an opening substantially void of any conductive diffusion barrier layer material.

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It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form an opening in the insulative material and being substantially void of any conductive diffusion barrier layer material in Pfister's device, in order to use to device in an application which requires contact to the gate electrode.

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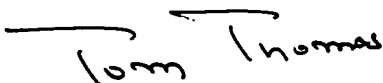
Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is (703) 308-8138. The Examiner is in the Office generally between the hours of 7 AM to 3 PM (Eastern Standard Time) Monday through Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached at (703) 308-2772.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is 308-0956

Ori Nadav

February 22, 2002


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